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09/963,270	09/24/2001	Alan H. Karp	10980982 -1	8394

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EXAMINER	
FOWLKES, ANDRE R	

ART UNIT	PAPER NUMBER
2192	

DATE MAILED: 02/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/963,270	KARP ET AL.	
	Examiner	Art Unit	
	Andre R. Fowlkes	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the amendment filed 11/28/05. Claims 1, 8 and 16 are amended. Claims 1-8 and 10-23 are pending.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-8 and 10-23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 1, 8 and 16 now include the limitation "resuming the execution of the object code without changing addresses of subsequent instructions in the object code". There is no support given from the original disclosure for this limitation. In the remarks, there is no listing of the page and line numbers from the specification in support of each change in the amended claims. Additionally, the examiner could not find this limitation in the specification. However, the specification does provide support for "resuming normal execution", as disclosed in the specification at p. 8:19-22. The examiner is interpreting the limitation "resuming the execution of the object code without changing addresses of subsequent instructions in

the object code" as meaning resuming normal execution to examine the application.

Accordingly, claims 2-7, 10-15 and 17-23 are also rejected. To overcome this rejection, the applicant may attempt to demonstrate that the original disclosure establishes that he or she was in possession of the amended subject matter by providing the page and line numbers, from the specification, in support of each of the new limitations in the claims.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-7, 16, 17 and 21-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Levine et al., (Levine), U.S. Patent No. 6,134,710.

As per claim 1, Levine discloses **a method for providing hint instructions to a processor** (col. 1:9-15, "the present invention relates to monitoring the performance of the operation of a computer processing system when executing an application program, ... and modifying the object code (by inserting hint instructions, e.g. pre-fetch instructions), on-line, in order to improve the operation of the application program in the processing system"), **comprising the steps of:**

- generating hint code that includes (i) a hint instruction in response to a set of object code to be executed by the processor (col. 2:28-38, "the present invention ... optimizes an application program by profiling the program to identify ... (instructions in) object code that result in long table walks or long cache misses, ... and (generating, then) inserting (hint code that includes hint) instructions into the object code to minimize the effects of long table walks and long cache misses by preloading or 'touching' an instruction or data"), **and (ii) a selected instruction to be removed from the set of object code,** (figs. 12A-12B and associated text, e.g. col. 14:22-30, show that the selected instruction, ("Instruction B"), is to be removed from the code. A branch instruction, ("Branch to Preload"), is inserted in place of the selected instruction such that the break instruction causes the processor to obtain and use the hint code (i.e. both the hint instruction ("Preload Cache"), and the selected instruction, ("Instruction B")),

- inserting a break instruction in place of the selected instruction in the object code such that the break instruction causes the processor to obtain and execute both the hint instruction and the selected instruction (col. 14:22-30, "FIG. 12A depicts an instruction sequence that contains an instruction, instruction E, that creates a long cache miss. FIG. 12B depicts a method of altering the code in real time by replacing instruction B with a branch instruction. The branch instruction branches to a preload or touch instruction (i.e. applicant's break instruction that causes the processor to obtain and execute an instruction) that preloads the instruction or data cache prior to the offending instruction E such that the required instruction or data is available in the appropriate cache when required by instruction E"),

- resuming execution of the object code without changing addresses of subsequent instructions in the object code (i.e. resuming normal execution) (FIG. 12B, shows the system executing instruction A, branching to execute the hint (preload) instruction and then resuming normal execution of instructions B and C, without changing the addresses of subsequent instructions).

As per claim 2, the rejection of claim 1 is incorporated, and further, Levine discloses that **the hint code further includes (iii) an instruction for the processor to resume execution of the set of object code** (fig. 12B and associated text, e.g. col. 14:22-30, shows that the hint code further includes an instruction for the processor to resume execution of the set of object code (i.e. the transition from instruction B to instruction C)").

As per claim 3, the rejection of claim 1 is incorporated, and further, Levine discloses **that the hint code adapts the set of object code so the set of object code can be executed by the processor** (col. 1:9-15, "the present invention relates to monitoring the performance of the operation of a computer processing system when executing an application program, ... and modifying the object code (by inserting hint instructions, e.g. pre-fetch instructions), on-line, in order to improve the operation of the application program in the processing system").

As per claim 4, the rejection of claim 1 is incorporated, and further, Levine discloses **loading the hint instruction into a hint register such that the break instruction causes the processor to obtain the hint instruction from the hint register and execute the hint instruction** (col. 2:40, "(hint instructions may be stored in) an optimized change file (and stored in a register, to be executed as a result of the break instruction)", and fig. 1 item 66, and associated text (e.g. col. 6:55-7:50), shows the "registers" which are loaded with and used to obtain hint instructions.

As per claim 5, the rejection of claim 4 is incorporated, and further, Levine discloses **loading the selected instruction into the hint register such that the break instruction causes the processor to obtain the selected instruction from the hint register and execute the selected instruction.** (col. 2:40, "(selected instructions may be stored in) an optimized change file (and stored in a register, to be executed as a

result of the break instruction)", and fig. 1 item 66, and associated text (e.g. col. 6:55-7:50), shows the "registers" which are loaded with and used to obtain selected instructions.

As per claim 6, the rejection of claim 4 is incorporated, and further, Levine discloses **loading an address into the hint register such that the break instruction causes the processor to load the hint register using the address** (col. 2:40, "(addresses may be stored in) an optimized change file (and stored in a register, to be loaded as a result of the break instruction)", and fig. 1, item 66, and associated text (e.g. col. 6:55-7:50) show the "registers".

As per claim 7, the rejection of claim 1 is incorporated, and further, Levine discloses **determining the hint instruction in response to a micro-architecture of the processor** (col. 1:9-15, "the present invention relates to monitoring the performance of the operation of a computer processing system, (composed of a specific micro-architecture), when executing an application program, ... and modifying the object code (by inserting hint instructions, e.g. pre-fetch instructions), on-line, in order to improve the operation of the application program in the processing system").

As per claim 16, this is another method version of the claimed method discussed above, in claim 2, wherein all claimed limitations have also been addressed and/or cited

as set forth above. For example, see Levine's adaptive method and system to minimize the effect of long cache misses, (col. 1:57-5:27).

As per claim 17, the rejection of claim 16 is incorporated and further, Levine discloses that **the hint instruction includes a pre-fetch instruction that causes the processor to fetch data from memory and write the data into a cache** (col. 2:33-35," inserting instructions (i.e. a pre-fetch hint instruction) into the object code that minimize the effects of ... long cache misses by preloading ... data (i.e. prefetch").

As per claim 21, the rejection of claim 16 is incorporated and further, Levine discloses **providing plural different types of hint instructions, wherein a type of hint instruction provided to the processor depends on functional capabilities of the processor** (col. 2:33-35," inserting instructions (i.e. a pre-fetch hint instruction) into the object code that minimize the effects of ... long cache misses by preloading ... data", and a different type of instruction, a branch prediction hint instruction, is provided for processors with the functional capabilities to support branch prediction, col. 14:22-30, "a ... touch instruction (i.e. a branch prediction instruction) that preloads the instruction ... cache prior to the offending instruction E such that the required instruction ... is available in the appropriate cache when required by instruction E").

As per claim 22, the rejection of claim 16 and further, Levine disclose that **a break instruction replaces a selected instruction at predetermined intervals** (col.

14:22-30, "a ... touch instruction (i.e. a branch prediction instruction) that preloads the instruction ... cache prior to the offending instruction E such that the required instruction ... is available in the appropriate cache when required by instruction E", and fig. 12 B shows how the break instruction replaces the selected instruction at a predetermined interval three instructions before the preloaded reference is needed).

As per claim 23, Levine also discloses such claimed limitations as addressed in claim 2, above.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 8-15 & 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levine et al., (Levine), U.S. Patent No. 6,134,710 in view of Eickemeyer et al., (Eickemeyer), U.S. Patent No. 5,377,336, (art made of record).

As per claim 8, this is a system version of the claimed method discussed above, in claim 1, wherein all claimed limitations have also been addressed and/or cited as set forth above, except for the limitation that the hint instruction **includes a branch**

prediction instruction. Levine doesn't explicitly disclose that **the hint instruction includes a branch prediction instruction.**

However, Eickemeyer, in an analogous environment, discloses that the hint instruction **includes a branch prediction instruction** (col. 2:61-62, "Another broad class of prefetching is instruction prefetching based on branch prediction").

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the teachings of Eickemeyer into the system of Levine to have the hint instruction include a branch prediction instruction. The modification would have been obvious because one of ordinary skill in the art would have wanted to include the well known and well document branch prediction instruction to increase the execution speed of code, (Eickemeyer col. 2:61-62).

As per claims 10-15, this is a system version of the claimed method discussed above, in claims 1-7, wherein all claimed limitations have also been addressed and/or cited as set forth above. For example, see the Levine/Eickemeyer combination, (Levine, col. 1:57-5:27 & Eickemeyer, col. 2:61-62).

As per claim 18, the rejection of claim 16 is incorporated and further, this is a method version of the claimed system discussed above, in claim 8, wherein all claimed limitations have also been addressed and/or cited as set forth above. For example, see the Levine/Eickemeyer combination, (Levine, col. 1:57-5:27 & Eickemeyer, col. 2:61-62).

7. Claims 19 & 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levine et al., (Levine), U.S. Patent No. 6,134,710 in view of Grimsrud et al., (Grimsrud), "Multiple Prefetch Adaptive Disk Caching", IEEE Transactions on Knowledge and Data Engineering Vol. 5, No. 1, February 1993.

As per claim 19, the rejection of claim 16 is incorporated and further, Levine discloses **adapting a number of hint instructions to increase instruction execution of the processor** (col. 2:28-38, "the present invention ... optimizes an application program by profiling the program to identify ... (instructions in) object code that result in long table walks or long cache misses, ... and (adapting a number of hint) instructions into the object code that minimize the effects of long table walks and long cache misses by preloading or 'touching' an instruction or data").

Levine doesn't explicitly disclose **providing plural hint instructions**.

However, Grimsrud, in an analogous environment, discloses **providing plural hint instructions** (p. 92 col. L:17, "multiple prefetching (i.e. plural hint instructions)").

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the teachings of Grimsrud into the system of Levine to **provide plural hint instructions**. The modification would have been obvious because one of ordinary skill in the art would have wanted to ensure that at least one hint instruction is executed for a memory reference even if the architecture is designed to drop one or more hint instructions for a memory reference.

As per claim 20, the rejection of claim 16 is incorporated and further, Levine discloses **adapting a number of hint instructions depending on a cache size of the processor** (col. 2:28-38, "the present invention ... optimizes an application program by profiling the program to identify ... (instructions in) object code that result in long table walks or long cache misses, ... and (adapting a number of hint) instructions into the object code that minimize the effects of long table walks and long cache misses by preloading or 'touching' an instruction or data").

Levine doesn't explicitly disclose **providing plural hint instructions**.

However, Grimsrud, in an analogous environment, discloses **providing plural hint instructions** (p. 92 col. L:17, "multiple prefetching (i.e. plural hint instructions)").

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the teachings of Grimsrud into the system of Levine to **provide plural hint instructions**. The modification would have been obvious because one of ordinary skill in the art would have wanted to ensure that at least one hint instruction is executed for a memory reference even if the architecture is designed to drop one or more hint instructions for a memory reference.

Response to Arguments

7. Applicants arguments have been considered but they are not persuasive.

In the remarks, the applicant has argued substantially that:

1) Nowhere does Levine teach inserting break instructions into the object code. By contrast, Levine teaches inserting branch instructions into the object code. Break instructions are very different from branch instructions, at p. 6:10-15

Examiner's response:

1) The examiner agrees that the accepted meaning of a break instruction is different from the accepted meaning of a branch instruction. However, in the specification and in claim 1, the applicant has defined the break instruction as an instruction that obtains and executes other instructions, similar to tasks executed by a conventional branch instruction. For example, applicants disclosure cites that "The break mechanism of the processor 10 may be implemented ... to branch to a predetermined address when a break instruction is executed", at p. 8:9-14. Accordingly, the Levine system performs all of the functions defined by applicant's break instruction.

In the remarks, the applicant has argued substantially that:

2) The cited art does not disclose that the processor resumes normal execution of the object code without changing addresses of subsequent instructions in the object code, at 6:28-7:3.

Examiner's response:

2) The examiner disagrees with applicant's characterization of the applied art. Levine does disclose that the processor resumes normal execution of the object code

without changing addresses of subsequent instructions in the object code, in figure 12B. Figure 12B, shows the system executing instruction A, branching to execute the hint (preload) instruction and then resuming normal execution of instructions B and C, without changing the addresses of subsequent instructions).

In the remarks, the applicant has argued substantially that:

3) Levine does not disclose a hint register, at p. 7:18-20.

Examiner's response:

3) The examiner disagrees with applicant's characterization of the applied art. Levine does disclose a hint register at col. 2:40 and col. 6:55-7:50, as disclosed in the above art rejection.

In the remarks, the applicant has argued substantially that:

4) Levine does not teach hint instructions, at p. 8:1-2.

Examiner's response:

4) The examiner disagrees with applicant's characterization of the applied art. Levine does disclose hint instructions in Figures 12A and 12B. Figures 12A-12B and associated text, e.g. col. 14:22-30, show that the selected instruction, ("Instruction B"), is to be removed from the code. A branch instruction, ("Branch to Preload"), is inserted in place of the selected instruction such that the break instruction causes the processor

to obtain and use the hint code (i.e. the hint instruction ("Preload Cache"), the selected instruction, ("Instruction B") and the instruction for the processor to resume normal execution of the set of object code (i.e. the transition from instruction B to instruction C)").

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre R. Fowlkes whose telephone number is (571) 272-3697. The examiner can normally be reached on Monday - Friday, 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571)272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TUAN DAM
SUPERVISORY PATENT EXAMINER

ARF